IN THE CLAIMS

Please amend the claims as shown below. Please cancel Claim 5 without prejudice. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) A circuit for providing power on reset functions and a plurality of functions for power system control for a microcontroller, comprising:

a first stage for performing power on reset functions and functions related to operational, post power on reset power stability;

a second stage for stimulating a reliable source of startup power during power on reset, wherein said second stage produces a first signal for forcing a switch mode pump to drive up voltage provided to said common power supply and a second signal forcing said microcontroller into a power on reset condition;

a bus for providing an interconnection with a processor; and

a processor providing dynamic control over said first stage.

2. (Original) The circuit as recited in Claim 1, wherein said first stage further comprises a power supply scaler for dividing a common power supply output into a plurality of divisional outputs.

3. (Original) The circuit as recited in Claim 2, wherein said power supply scaler comprises:

a precision divider of said common power supply output having a plurality of taps, each providing an independent, distinct division of said common supply output;

a matrix of multiplexers and registers for selecting from said plurality of taps and correspondingly configuring said plurality of divisional outputs.

4. (Original) The circuit as recited in Claim 3, wherein said matrix of multiplexers and registers selects from said plurality of taps, correspondingly configuring said plurality of divisional outputs under control of said processor.

5. (Cancelled)

6. (Original) The circuit as recited in Claim 1, wherein said plurality of power stability functions comprise:

a) a power on reset function;

b) a power supply monitoring function;

c) a control function for said common supply source; and

d) auxiliary functions.

7. (Original) The circuit as recited in Claim 6, wherein said power on reset function operates at a fixed voltage level.

8. (Original) The circuit as recited in Claim 6, wherein said power supply monitoring function further comprises a power supply health signal.

9. (Currently Amended) The circuit as recited in Claim 6, wherein said control function for said common supply source further comprises a signal for controlling said switch mode pump ~~control signal~~.

10. (Original) The circuit as recited in Claim 6, wherein said power stability functions are, selectively, programmable, and operable at a fixed voltage.

11. (Original) The circuit as recited in Claim 6, wherein one of said auxiliary functions further comprises a trip signal for a flash memory.

12. (Currently Amended) A circuit for providing power on reset functions and a plurality of functions power system control for a microcontroller, comprising:

a) a power supply scaler for receiving an input voltage from a switched mode pump common supply source, dividing said input voltage into a plurality of output scaler voltages;

b) a source of a precision reference voltage for comparison to said plurality of scaler output voltages;

c) a plurality of comparators for comparing said precision reference voltage and said plurality of scaler output voltages;

d) a qualifier for validating said precision reference voltage;

e) an initial power reference source for providing a reliable voltage reference while energizing said microcontroller; and

f) a logic gate for asserting a reset condition on said microcontroller.

13. (Original) The circuit as recited in Claim 12, wherein said power supply scaler further comprises:

a1) a variable path divider of said input voltage; and

a2) a multiplexer and register matrix.

14. (Original) The circuit as recited in Claim 13, wherein said variable path voltage divider comprises an array of resistors.

15. (Original) The circuit as recited in Claim 13, wherein said variable path voltage divider comprises an array of capacitors.

16. (Original) The circuit as recited in Claim 13, wherein said variable path voltage divider comprises an array of charge-sensing devices.

17. (Original) The circuit as recited in Claim 13, wherein said variable path voltage divider comprises an array of metal oxide semiconductor field effect transistors.

18. (Original) The circuit as recited in Claim 12, wherein said variable path voltage divider comprises an array of current sensing devices.

19. (Original) The circuit as recited in Claim 12, wherein said precision reference voltage is independent of said input voltage, and is monitored by a precision reference voltage monitor, said precision reference voltage monitor generating a precision reference voltage validity signal, said precision reference voltage validity signal comprising a zero state when said precision reference voltage is valid, and a non-zero state when said precision reference voltage is not valid.

20. (Original) The circuit as recited in Claim 18, wherein said plurality of comparators each compare a plurality of output voltages from said power supply scaler, each of said output voltages individually, to said precision voltage reference, and correspondingly generate one of a plurality of power stability signals, said plurality of power stability signals comprising:

a) a power on reset signal;

b) a power supply monitoring signal;

c) a control signal for said switch mode pump; and

d) auxiliary signals.

21. (Original) The circuit as recited in Claim 20 said source of an initial power reference source further comprises:

e1) an initial voltage generator; and

e2) a initial power comparator, said initial power comparator sensing an input generated by said initial voltage generator and said common supply source, comparing them one to another, and generating an initial power comparator output; said initial power comparator output initially driving a switch mode pump to raise voltage of said common supply source.

22. (Original) The circuit as recited in Claim 21, wherein said logic gate comprises an OR gate, said OR gate generating an OR gate output wherein said OR gate output, in one state initiated by any non-zero value of a plurality of inputs, asserts a power on reset condition, and in another state by all zero values of said inputs, de-asserts said power on reset condition, said inputs comprising:

f1) said power on reset signal;

f2) said initial power comparator output; and

f3) said precision reference voltage validity signal.

23. (Currently Amended) In a microcontroller having a power supply ~~fed by a switch mode pump~~, a method of performing power stability functions utilizing a power on reset circuit, during startup and post-startup operations, said method comprising: ~~the steps of:~~

a) performing a power on reset function during startup wherein said power supply is fed by a switched mode pump; and

b) utilizing said power on reset circuit, during post-startup operation to:

perform power on reset functions upon trip;

monitor a condition of said power supply;

control said switch mode pump; and

provide auxiliary control, indication, and memory protective trip.